IN THE CLAIMS

1-30. (Cancelled)

31. (New) A system comprising:

a graphics controller coupled to a graphics memory; and

a compression process invoked by the graphics controller upon receipt of an idle notification to cause the graphics controller to compress an idle graphics frame for storage into the graphics memory.

32. (New) The system of claim 31, wherein the compression process further causes the graphics controller to represent a pixel value in the idle graphics frame with a code.

33. (New) The system of claim 32, wherein the code requires fewer bits than the pixel value.

34. (New) The system of claim 32, wherein the compression process further causes the graphics controller to select the pixel value based on a number of occurrences of the pixel value in the idle graphics frame.

35. (New) The system of claim 34, wherein the compression process further cause the graphics controller to select the pixel value if the number of occurrences satisfies a threshold.

36. (New) The system of claim 35, wherein the threshold is a percentage of a total number of occurrences of pixel values in the idle graphics frame.

37. (New) The system of claim 34, wherein the compression process further causes the graphics controller to evaluate two idle graphics frames to determine the number of occurrences.

38. (New) The system of claim 32, wherein the compression process further causes the graphics controller to encode a compressed idle graphics frame to identify the code within the compressed idle graphic frame.

39. (New) The system of claim 31, wherein the compression process further causes the graphics controller to uncompress a compressed idle graphics frame retrieved from graphics memory.

40. (New) The system of claim 39, wherein the pixel value is represented by a code in the compressed idle graphics frame and the graphics controller replaces the code with the pixel value when uncompressing the compressed idle graphics frame.

41. (New) The system of claim 40, wherein the compressed idle graphics frame is encoded to identify the code within the compressed idle graphics frame and the graphics

controller decodes the compressed idle graphics frame when uncompressing the compressed idle graphics frame.

42. (New) The system of claim 31, wherein the compression process further causes the graphics process to compress a non-idle graphics frame upon receiving an override indicator.

43. (New) The system of claim 31, wherein the system further comprises a processor coupled to the graphics controller through a system bus, the processor executing a display driver to send the idle graphics frame and the idle notification to the graphics controller.

44. (New) The system of claim 43, wherein the system further comprises a system memory coupled to the processor through the system bus, the system memory comprising the graphics memory.

45. (New) The system of claim 43, wherein the system further comprises a display coupled to the graphics controller to display graphics frames stored in the graphics memory.